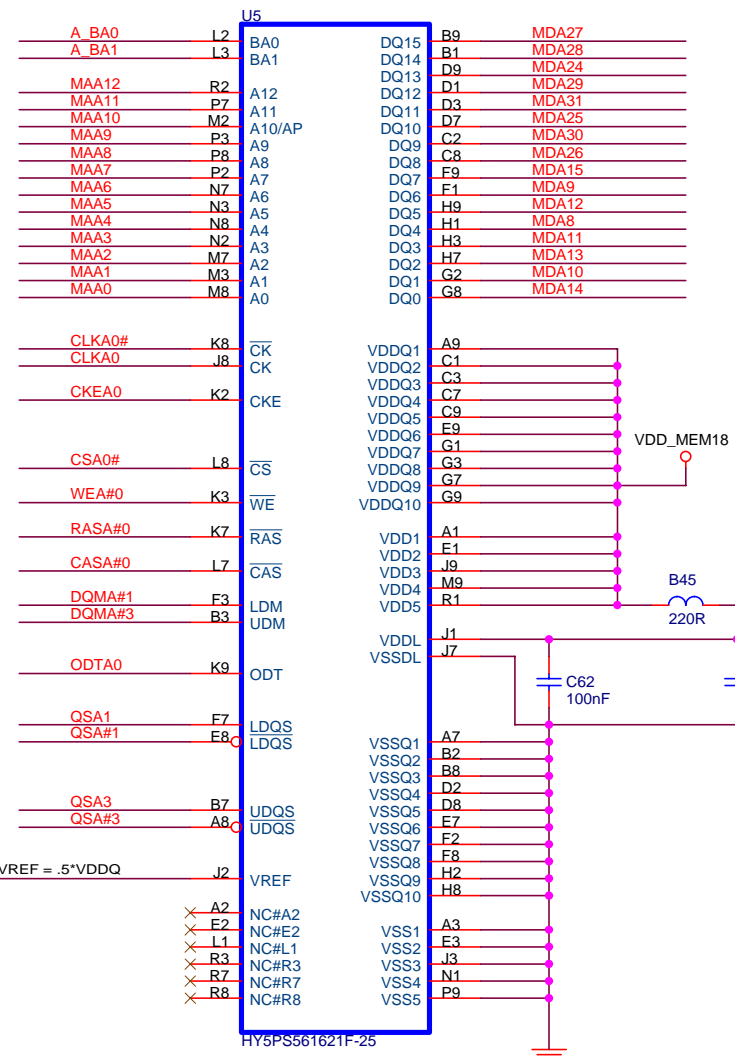
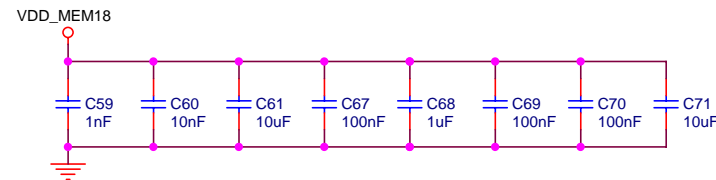
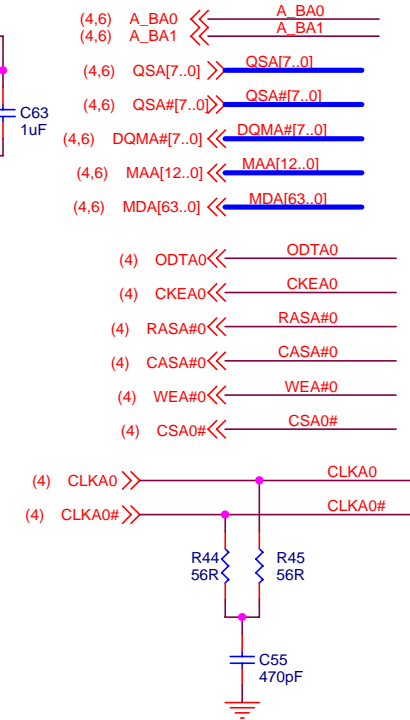
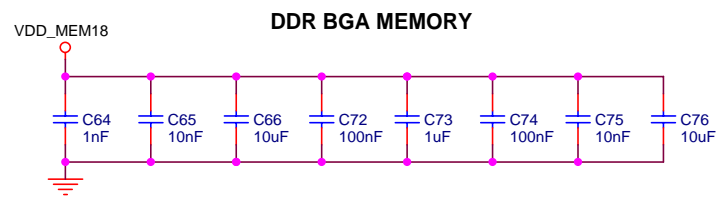


DDR2 BGA MEMORY



DDR BGA MEMORY



CHAN A RANK 0 DDR2 BGA MEMORY

<Variant Name>

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Markham, Ontario  
Canada, L3T 7X6  
(905) 882-2600

Title: AXIOM-AFFII M56-P A RANK DDR2

Size: Custom

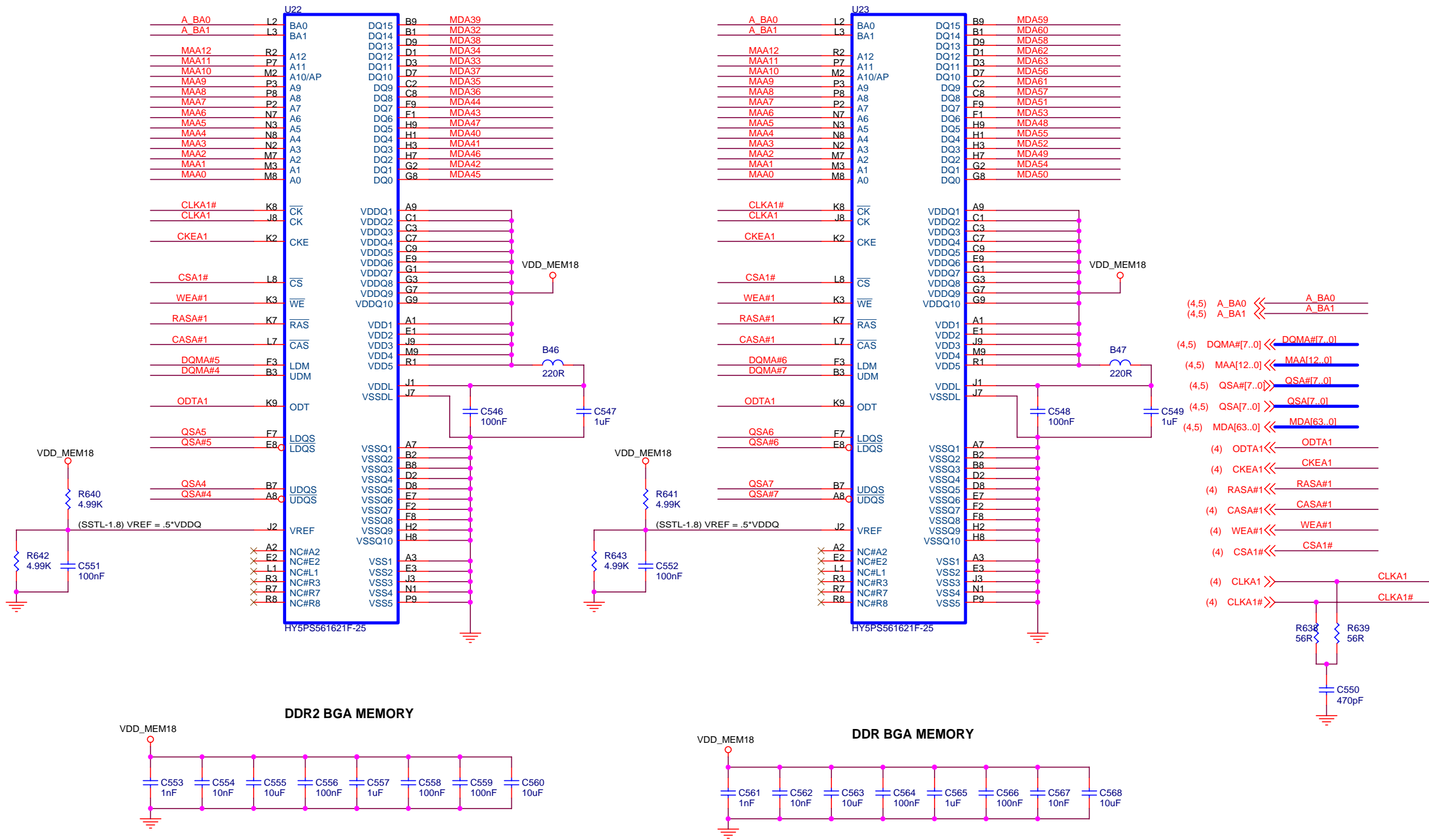
Document Number: 105-A828XX-00A

Date: Tuesday, October 18, 2005

Sheet: 5 of 14

Rev: 0



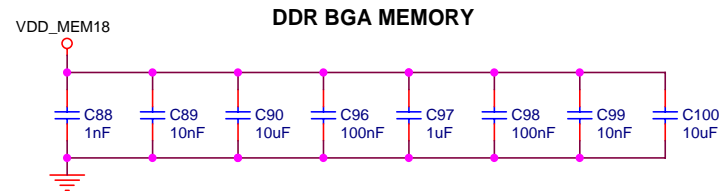
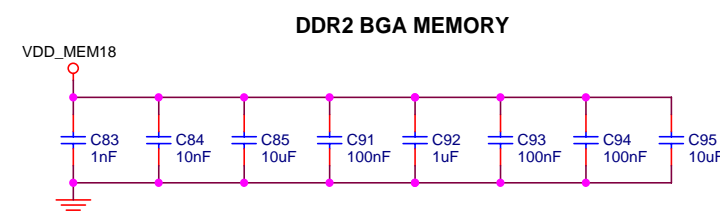
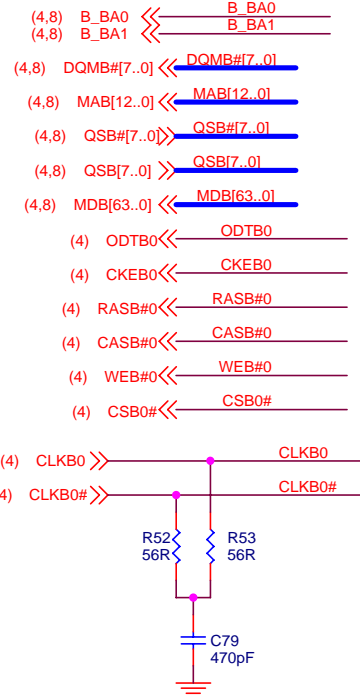
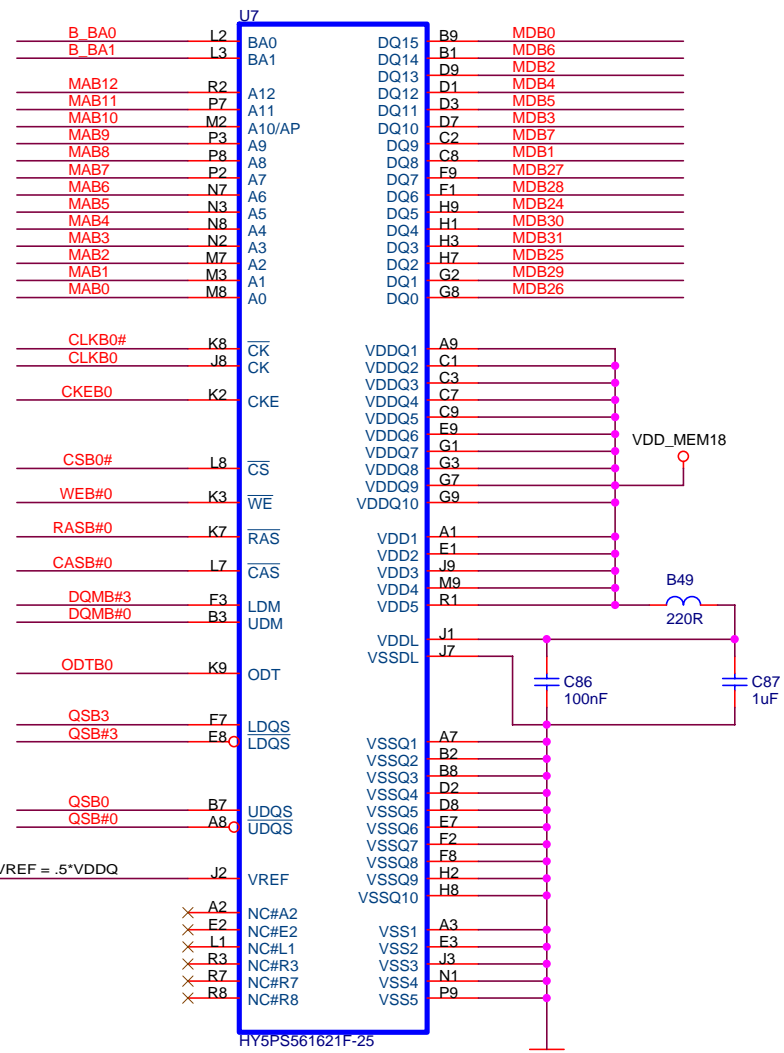
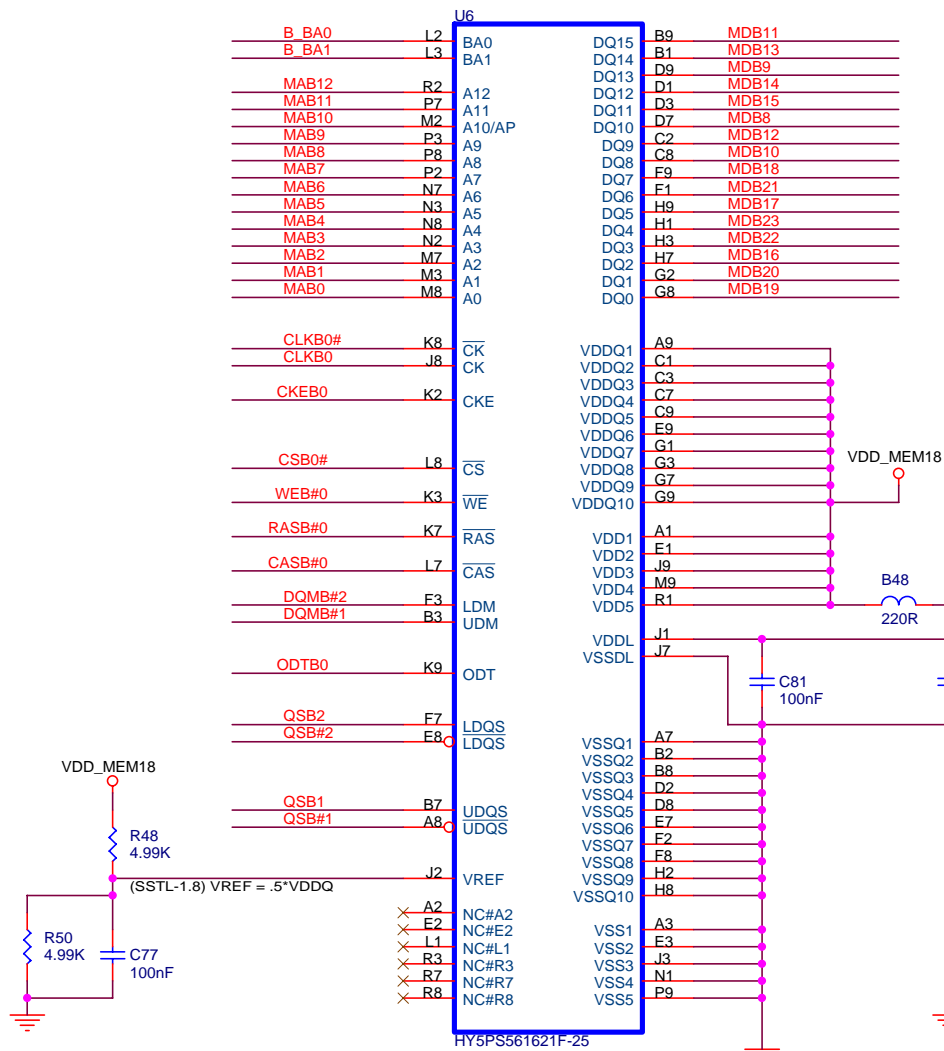


CHAN B RANK 0 DDR2 BGA MEMORY

<Variant Name>

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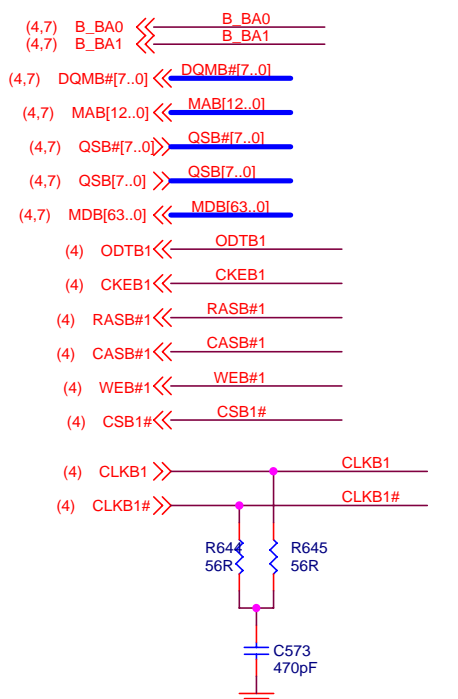
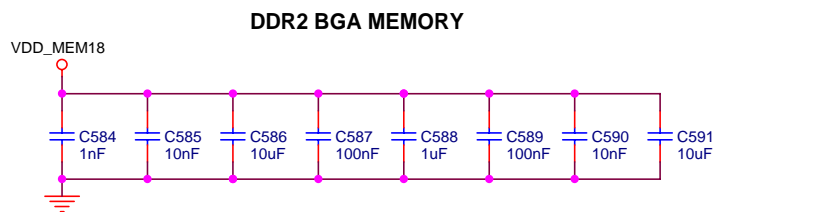
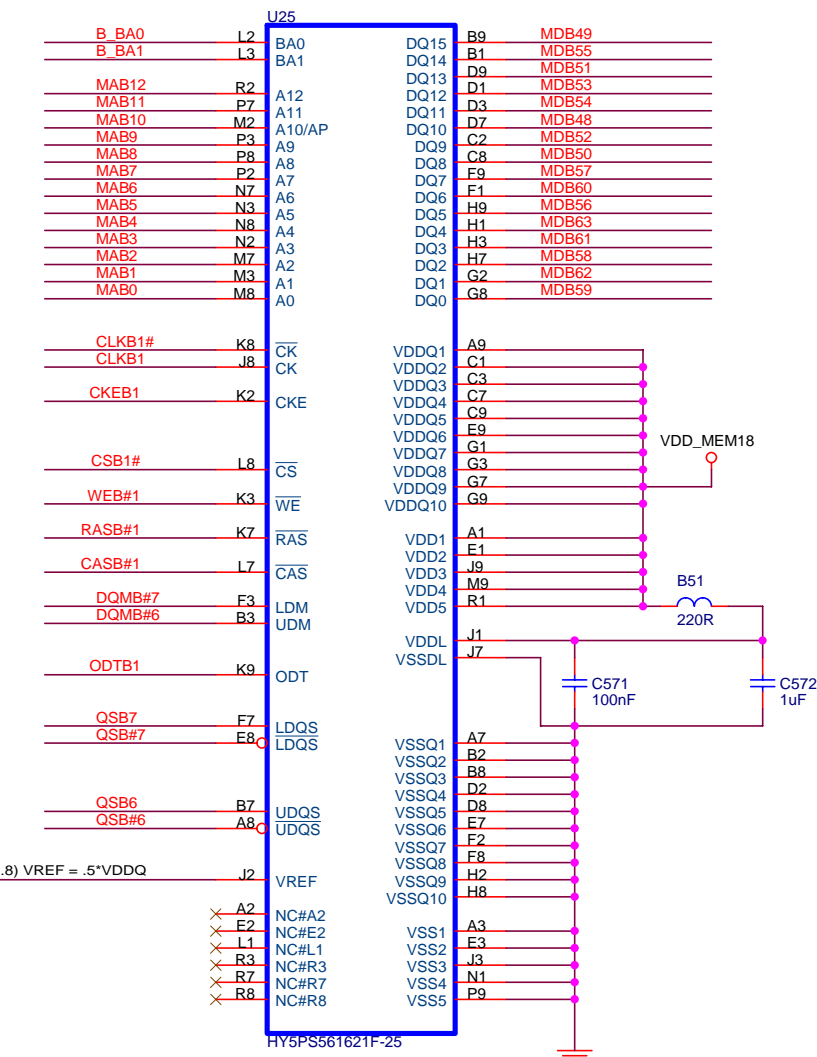
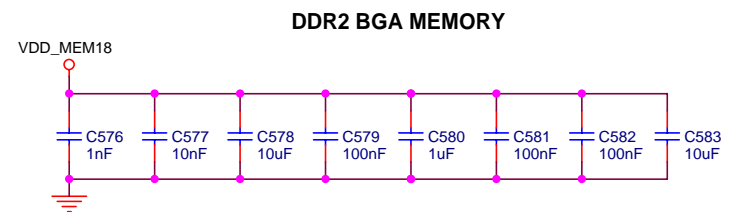
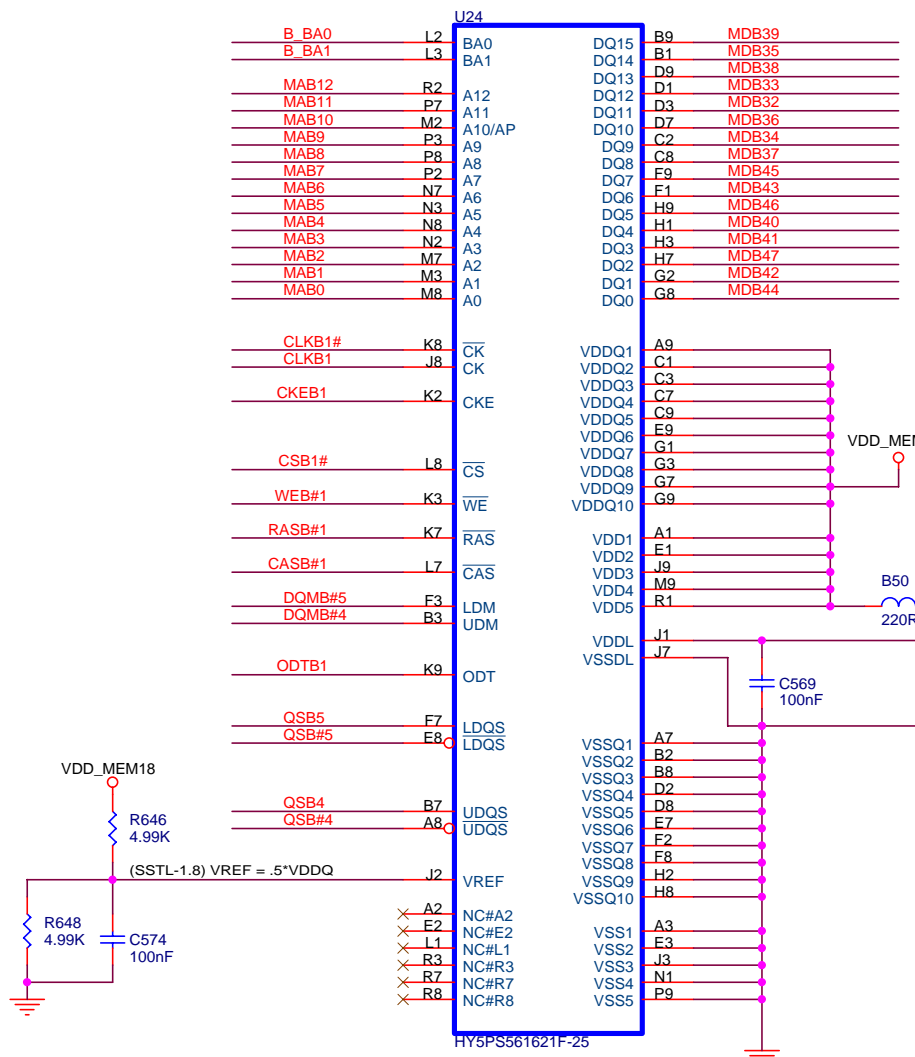
Title	AXIOM-AFFII M56-P A RANK DDR2		
Size	Document Number	105-A828XX-00A	Rev
Custpm			0
Date:	Tuesday, October 18, 2005	Sheet	6 of 14



CHAN C RANK0 DDR2 BGA MEMORY


<Variant Name>

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Title		AXIOM-AFFII M56-P A RANK DDR2	
Size	Document Number	105-A828XX-00A	Rev 0
Custpm	Date:	Tuesday, October 18, 2005	Sheet 7 of 14



CHAN D RANK0 DDR2 BGA MEMORY

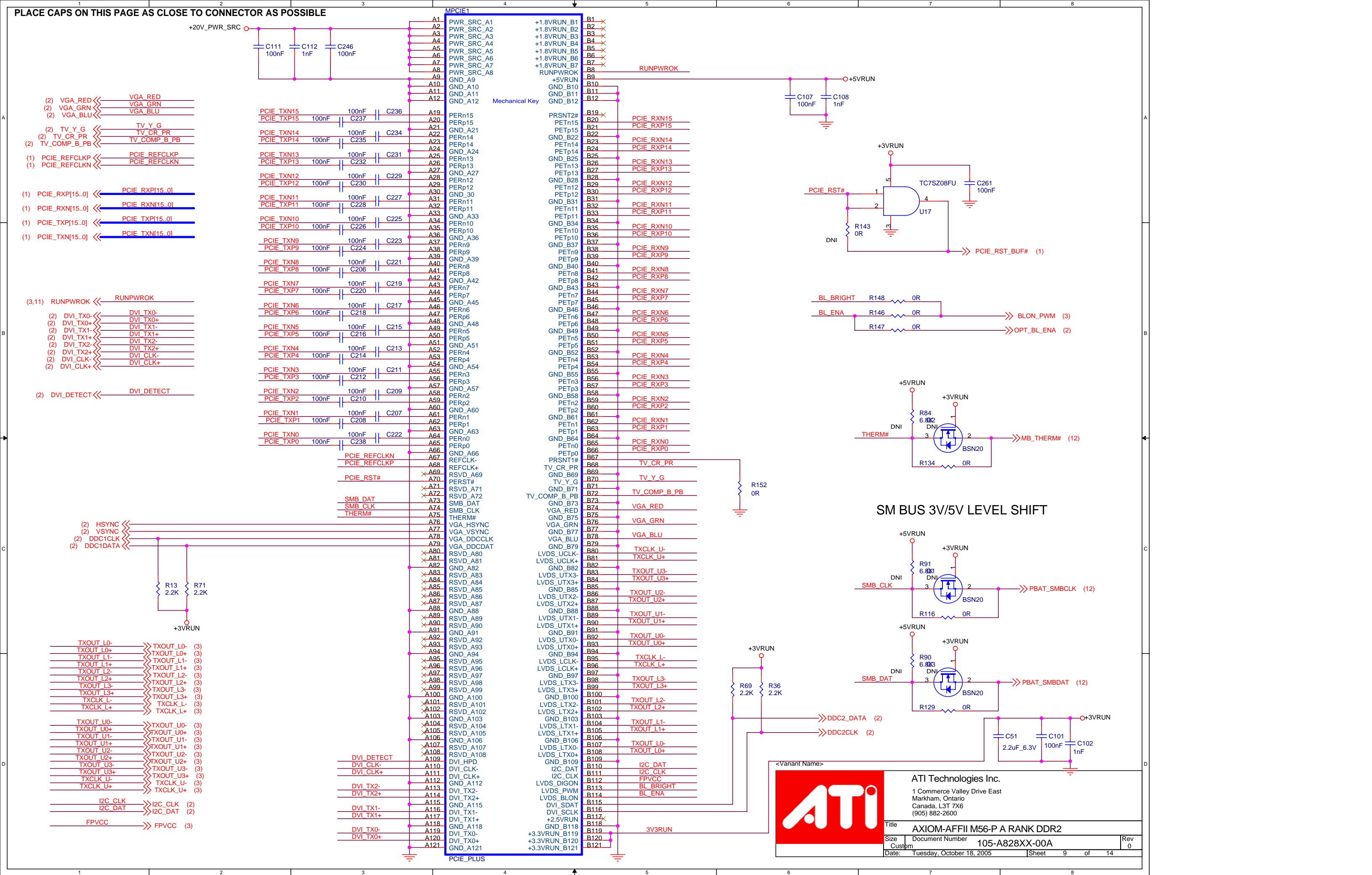
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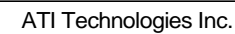
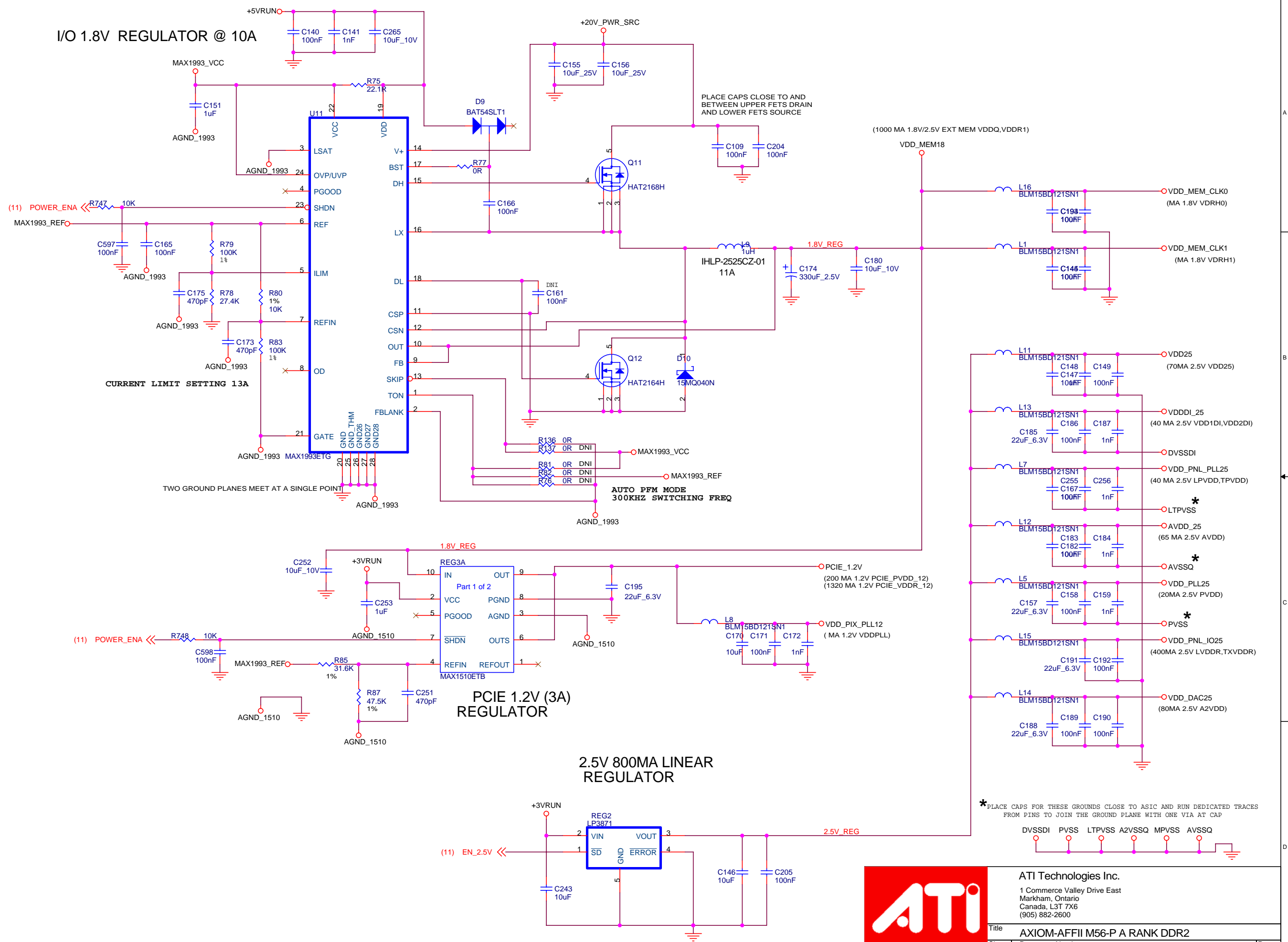


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Title		AXIOM-AFFII M56-P A RANK DDR2	
Size	Document Number	105-A828XX-00A	Rev 0
Custpm	Date:	Tuesday, October 18, 2005	Sheet 8 of 14







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Title				AXIOM-AFFII M56-P A RANK DDR2			
Size B		Document Number					Rev
		105-A828XX-00A					0
Date:		Tuesday, October 18, 2005			Sheet		10 of 14

CORE 1.0/1.15V REGULATOR @ 11A

INDUCTOR SATURATION PROTECTION DISABLED  
OVP, UVP AND DISCHARGE MODE ENABLED

(10) POWER\_ENA << +3VRUN R144 0R  
(3,9) RUNPWOK << DNI R145 0R

CURRENT LIMIT SETTING 13A  
Ra AND Rb = 75.0K FOR 1.0V LOW WITH POW\_SW(GATE) INPUT HIGH  
Ra AND Rb = 75.0K AND Rc = 43.2K FOR 1.22V HIGH WITH POW\_SW(GATE) INPUT LOW

(2) POW\_SW >>

TWO GROUND PLANES MEET AT A SINGLE POINT

CONNECT SKIP TO GND FOR AUTO PFM MODE - BOM DEFAULT  
CONNECT SKIP TO VCC FOR FORCED PWM MODE

CONNECT TON TO VCC FOR 200KHZ  
NO CONNECT TON FOR 300KHZ  
CONNECT TON TO REF FOR 450KHZ  
CONNECT TON TO AGND FOR 600KHZ -BOM DEFAULT

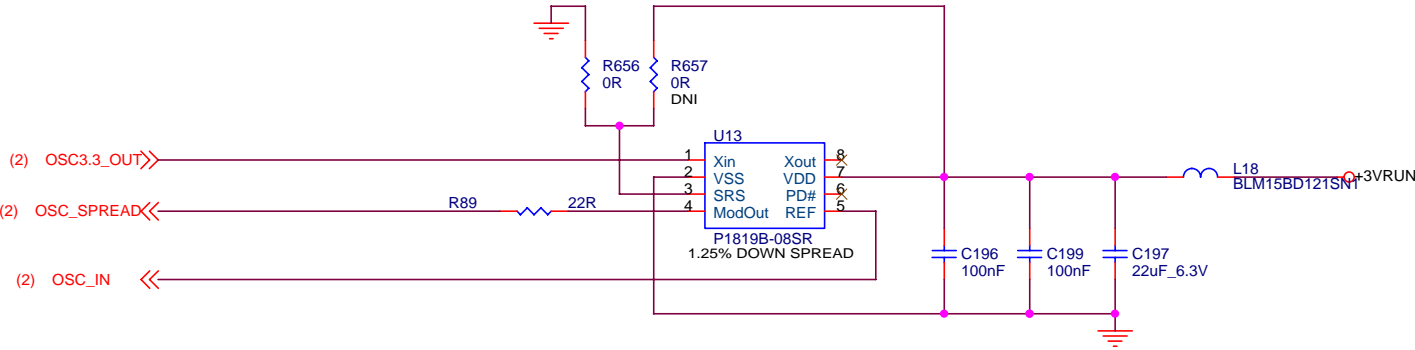
CONNECT FBLANK TO VCC FOR 140US tFBLANK FAULT BLANKING ENABLED  
NO CONNECT FBLANK FOR 90US tFBLANK FAULT BLANKING ENABLED - BOM DEFAULT  
CONNECT FBLANK TO REF FOR 40US tFBLANK FAULT BLANKING ENABLED  
CONNECT FBLANK TO GND FOR 90US tFBLANK FAULT BLANKING DISABLED



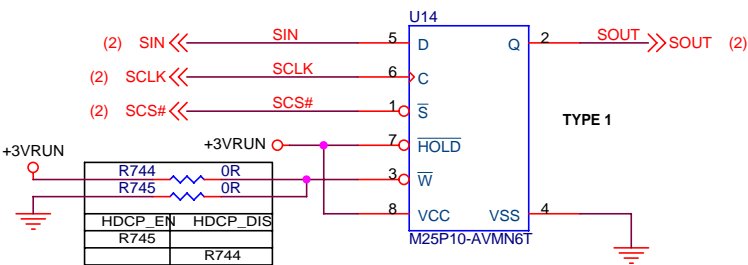
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Title		AXIOM-AFFII M56-P A RANK DDR2	
Size	Document Number	105-A828XX-00A	Rev
Custom			0
Date:	Tuesday, October 18, 2005	Sheet	11 of 14

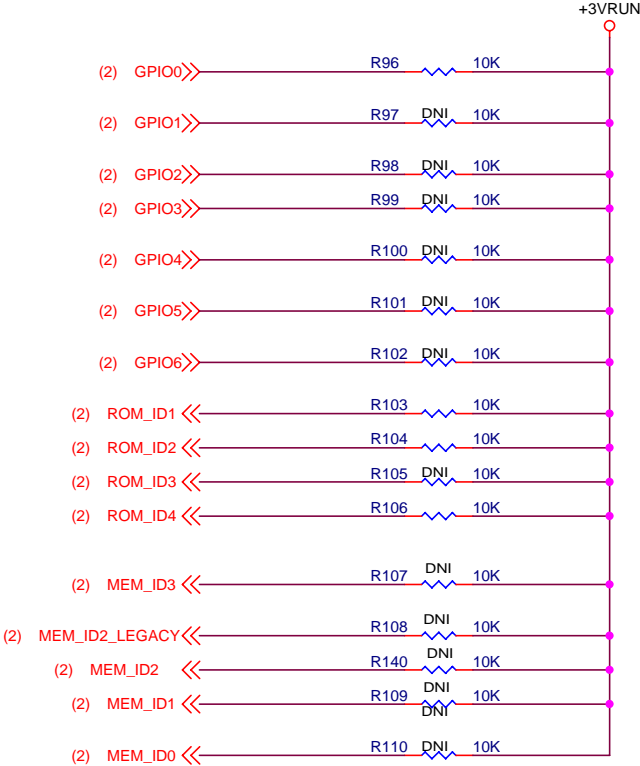
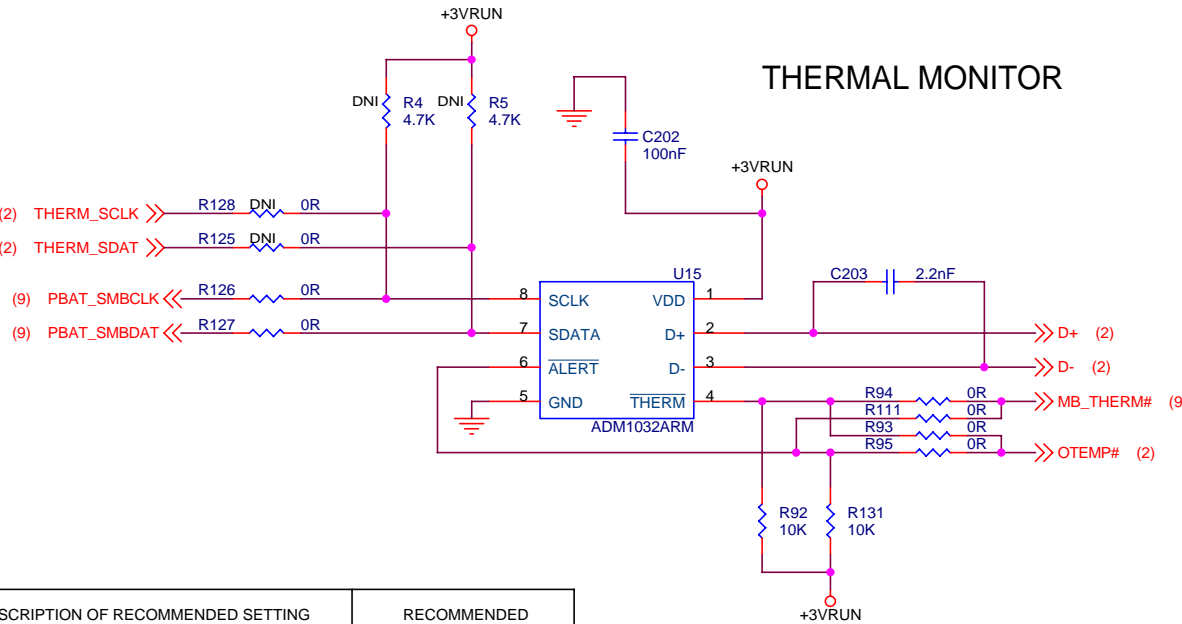
MEMORY CLOCK SPREAD SPECTRUM



FLASH ROM



THERMAL MONITOR



STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	Full swing	10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE - SETTING DEPENDS ON CHIPSET SEE M2X DATABOOKS	TBD
STRAP_PCIE_MODE	GPIO(3:2)	PCI-EXPRESS 1.0A MODE	DO NOT INSTALL 10K RESISTORS
STRAP_REVERSE_LANES	GPIO4	REVERSE PCIE LANES -NON REVERSED	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY	DO NOT INSTALL 10K RESISTORS
STRAP_CM_RANGE	GPIO6	CM RANGE - NORMAL	DO NOT INSTALL 10K RESISTORS
ROMIDCFG(3:0)	ROMID (4:1)	SERIAL FLASH ROM TYPE SELECT - SERIAL M25P10 ROM	1011
MEM_TYPE	MEMID (3:0)	TBD	TBD

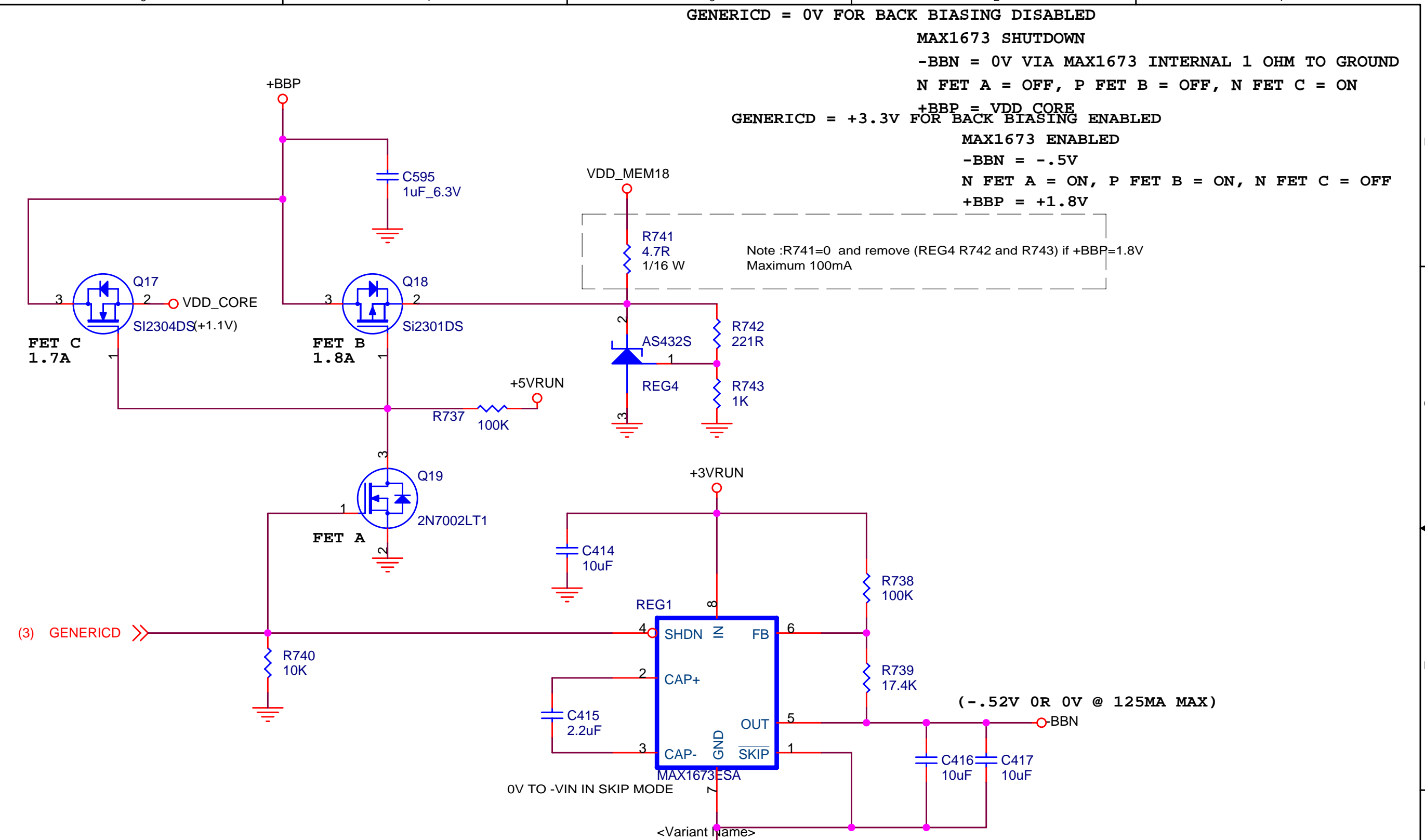
<Variant Name>



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Title	AXIOM-AFFII M56-P A RANK DDR2		
Size	Document Number	105-A828XX-00A	Rev 0
Custom	Date:	Tuesday, October 18, 2005	Sheet 12 of 14



GENERICD = 0V FOR BACK BIASING DISABLED

MAX1673 SHUTDOWN

-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND

N FET A = OFF, P FET B = OFF, N FET C = ON

GENERICD = +3.3V FOR BACK BIASING ENABLED

MAX1673 ENABLED

-BBN = -.5V

N FET A = ON, P FET B = ON, N FET C = OFF

+BBP = +1.8V

Note :R741=0 and remove (REG4 R742 and R743) if +BBP=1.8V  
Maximum 100mA

(3) GENERICD >>

(-.52V 0R 0V @ 125MA MAX)

0V TO -VIN IN SKIP MODE

<Variant Name>



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Title			AXIOM-AFFII M56-P A RANK DDR2	
Size	Document Number		105-A828XX-00A	
A			Rev 0	
Date:	Tuesday, October 18, 2005		Sheet	13 of 14





Title	Schematic No.	Date:
AXIOM-AFFII M56-P A RANK DDR2	105-A828XX-00A	Tuesday, October 18, 2005

REVISION HISTORY	Rev 0
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Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	12/08/05	PROTOTYPE BASED ON 105-A623XX-00A WITH FOLLOWING CHANGES: - CHANGE TO EIGHT PIECES OF DDR2 MEMORY -ADD BBP/BBN CIRCUIT .
1	00B	17/10/2005	1. Add R746 and C596 on page 3 2. Add R747 and C597 on page 10 3. Add R748 and C598 on page 10 4. Shift R33 to U9.4 on page 11